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 RAMBUS INC.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RAMBUS INC.,

 Plaintiff,

 v.
 LSI CORPORATION,

 Defendant.

Case No. 3:10-cv-05446 RS

**RAMBUS INC.'S OPENING CLAIM
 CONSTRUCTION BRIEF**

Date: August 29, 2012
 Time: 10:00 a.m.
 Judge: Hon. Richard Seeborg
 Courtroom 3, 17th Floor

RAMBUS INC.,

 Plaintiff,

 v.
 STMICROELECTRONICS N.V.;
 STMICROELECTRONICS INC.,

 Defendants.

Case No. 3:10-cv-05449 RS

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1 **I. INTRODUCTION**

2 In their Joint Claim Construction and Prehearing Statement, the parties identified ten
3 terms whose construction, they agreed, will be most significant to the resolution of these cases.
4 *LSI* Dkt. # 95, at 2. Six of these terms—“external clock signal,” “operation code,” “precharge
5 information,” “representative of,” “sample(s)/sampled/sampling,” and “synchronously with
6 respect to”—were previously construed by Judge Whyte in prior litigation involving some of the
7 same patents at issue here.¹ With respect to all six terms, Rambus here proposes that the Court
8 follow Judge Whyte’s well-reasoned constructions. In the case of two other terms—“clock
9 signal” and “synchronous dynamic random access memory device”—Judge Whyte construed
10 closely related terms and, again, Rambus urges the Court to follow Judge Whyte’s reasoning in
11 construing the terms at issue here. The final two terms—“controller/controller device” and
12 “register”—were not previously construed by Judge Whyte because Rambus and its litigation
13 opponents, sophisticated memory chip manufacturers, had agreed on the constructions of these
14 straightforward terms, and Rambus proposes that the Court adopt these previously agreed
15 constructions here.

16 By contrast Defendants urge the Court to depart from Judge Whyte’s reasoning on all but
17 one of the eight terms that implicate Judge Whyte’s prior constructions. With respect to the one
18 exception—“precharge information”—the Defendants propose that the Court adopt an early
19 construction of Judge Whyte’s rather than his most recent construction of the term. As to the
20 remaining two terms, the Defendants reject the previously agreed constructions and ask the Court
21 to adopt new constructions.

22 As set forth below, the prior constructions of the claim terms at issue—whether ruled on
23 by Judge Whyte or agreed to by Rambus’s litigation opponents—are fully supported by the
24 intrinsic and extrinsic evidence and capture the understanding that a person of ordinary skill in the
25 art would have had of these terms at the time Rambus’s original patent application was filed. It

27 ¹ “Representative of” was construed by Judge Whyte in the context of phrases containing that
28 term.

seems highly unlikely that Judge Whyte would have erred in his construction of all these terms, or that Rambus's technically savvy prior litigation opponents would have agreed to constructions of terms that varied from the understanding of a person of ordinary skill in the art. Defendants' rejection of all these prior constructions suggests that Defendants' proposed constructions of the terms at issue are motivated not by a consideration of how one of ordinary skill in the art would have understood the terms, but by some perceived tactical advantage in this litigation. The Court should reject Defendants' unsupported proposed constructions and adopt Rambus's proposed constructions of the claim terms at issue.

II. TECHNOLOGY BACKGROUND

A. DRAM Memory Systems

The inventions described in the specification of the Farmwald/Horowitz patents-in-suit² relate to improving the speed and efficiency of the communication between memory controllers and different types of memory devices, including Dynamic Random Access Memory (DRAM), Static Random Access Memory (SRAM), and Read Only Memory (ROM) devices. '916 patent, col. 6:16-20. Because the accused devices in this case are DRAM controllers, this background will focus on the applicability of the patented inventions to DRAM memory system technology.

Numerous types of electronics devices, including computers, DVD players, set-top boxes, hard-drive controllers, GPS devices, and a host of others, use DRAM chips to store information. The DRAMs are used by the processor—the “brains” of the device—as a storage area for data, calculation results, and program instructions, drawing on this storage as necessary to perform the tasks required by the programs. A memory controller acts as a sort of middle-man, sending data

² The Farmwald/Horowitz patents currently at issue in this litigation all claim priority to an original application, Serial No. 07/510,898 (the '898 application), which was filed by Professors Michael Farmwald and Mark Horowitz, the founders of Rambus, on April 18, 1990. Consequently, the patents share essentially the same written description and drawings. For simplicity, since the patents do have minor differences in column and line numbering, Rambus's references to the specification of the patents will be to U.S. Patent No. 6,426,916 (the "'916 patent"). A copy of the '916 patent is attached as Exhibit A to the Declaration of Peter A. Detre in Support of Rambus Inc.'s Opening Claim Construction Brief (“Detre Decl.”).

1 and instructions to the DRAMs to store and retrieve the information required by the processor. At
 2 the time of the filing of the '898 application, memory controllers were, generally, stand-alone
 3 chips, but today memory controllers are often integrated with the processor on the same chip.
 4 The specific type of memory controllers involved in this case are those that control certain types
 5 of SDRAM (Synchronous DRAM) .

6 The DRAM memory systems at issue generally reside on a printed circuit board and
 7 consists of a DRAM memory controller, often integrated with a processor as described above, and
 8 one or more DRAMs connected to the controller by means of a set of traces (conductive paths)
 9 called the "memory bus."

10 1. DRAMs

11 Each DRAM chip is composed of two parts: the memory array and the peripheral
 12 circuitry that interfaces with the DRAM memory controller. *See, e.g.*, '916 patent, Fig. 1
 13 (showing "RAM ARRAY" and peripheral circuitry). The memory array (sometimes referred to
 14 as the "memory core") of a DRAM is comprised of numerous cells, or storage locations, each
 15 made up of a capacitor and a transistor. Each DRAM cell can hold one "bit" (binary digit) of
 16 information, that is, it can distinguish between a "0" and a "1" depending on whether the
 17 capacitor is charged or not. Because capacitors lose their charge over time, it is necessary to
 18 recharge, or refresh, the cell periodically to avoid the loss of information. It is this need to refresh
 19 a DRAM that is responsible for the "dynamic" part of its name, and which distinguishes it from
 20 Static RAM (SRAM). (The more complex circuitry of an SRAM holds its charge so there is no
 21 need to refresh.)

22 DRAM cells are combined into a large array that is used to store vast amounts of
 23 information. The cells are organized in terms of rows and columns, with each cell having a
 24 specific row/column reference (address location). The memory controller can access (read
 25 from/write to) each cell by specifying the address at which it is located.³

26 ³ When the information stored in a DRAM cell is to be read, the controller transmits the
 27 appropriate row and column address to the DRAM. First, the appropriate word line (row) in the
 28 DRAM is activated and the small voltage differences representing the information stored in that
 (continued...)

1 The density of DRAMs has increased dramatically since the 1970s when DRAMs were
 2 first introduced. The first DRAMs contained 1,024 bits (one kilobit or 1 Kb); today, two and four
 3 gigabit (a gigabit being, approximately, one billion bits) DRAMs are typical, with eight gigabit
 4 DRAMs becoming more readily available. Aside from the dramatic increases in density over
 5 time, the memory arrays of DRAMs have changed little since DRAMs first became available.

6 2. DRAM Controllers

7 The increased density of DRAMs does nothing, however, to make the transfer of data into
 8 and out of those DRAMs faster and more efficient. Much of the improvement in DRAM
 9 performance over time has come as the result of changes to DRAM controllers and corresponding
 10 changes to the DRAM's peripheral circuitry that interfaces with the controller. Rambus's patents
 11 apply to both sides of this interface—the DRAM controller and the peripheral circuitry of the
 12 DRAMs themselves—and are directed at improving the speed and efficiency of communication
 13 between the controller and the DRAMs.

14 Prior to the 1990s, DRAM memory systems operated asynchronously. In other words,
 15 read and write operations were conducted without reference to a “clock,” that is, a periodic signal
 16 that transitions from a low to a high voltage and back (akin to a metronome). DRAM controllers
 17 accessed the DRAMs using a so-called “RAS/CAS” interface (with “RAS” standing for Row
 18 Address Strobe and “CAS” for Column Address Strobe).⁴ When information at a particular
 19 memory location was to be read, the controller would transmit the row address to the DRAM as
 20 well as a control signal called /RAS (pronounced RAS-bar) whose transition would latch the row
 21 address from the address pins. Once the corresponding word line was activated, the controller
 22 would transmit the column address to the DRAM along with the /CAS (pronounced CAS-bar)
 23 control signal, whose transition would latch in the column address from the address pins. The

24 (...continued)
 25 row of memory cells are amplified by so-called “sense amplifiers.” Next, the high or low voltage,
 26 representing a “1” or “0,” in the appropriate column is transferred from the corresponding sense
 27 amplifier to an input/output pin of the DRAM from where it can be read by the controller.
 28 Information from an outside source can, likewise, be written to a DRAM by the controller.

⁴ A “strobe” is a signal that can be used as a timing reference for certain operations, but that is not periodic—i.e., does not repeat at regular intervals—like a clock signal.

1 DRAM would then extract the information from the addressed memory cell and transfer the
2 appropriate voltage (representing the information) to the DRAM's input/output pins, from where
3 the information would be transferred over the memory bus to the controller. Write operations
4 were executed similarly, with the controller sending the data, as well as the row and column
5 address of the target location, to the DRAM for storage. Another control signal was used to
6 distinguish between read and write operations. In order to execute an operation correctly, the
7 control signals had to be sent in the correct sequence and held for the duration of the operation.

8 The accused devices are controllers of certain memory devices that were standardized by a
9 standard-setting organization known as JEDEC beginning in the early 1990s with SDRAMs
10 (Synchronous DRAMs), and following in subsequent years through the present with DDR
11 SDRAMs (Double Data Rate SDRAMs), DDR2 SDRAMs, DDR3 SDRAMs, LPDDR SDRAMs
12 (Low Power DDR SDRAMs) and LPDDR2 SDRAMs. Unlike conventional DRAMs, SDRAMs
13 and the follow-on devices operate synchronously: interface operations, such as reads and writes,
14 are conducted with reference to an external clock signal received by the DRAM. While the
15 control signals used in SDRAM retain the names of the control signals used in older DRAMs, the
16 DRAMs do not sense the transitions of these signals and the signals need not be held for the
17 duration of an operation; rather, a command sent by the controller to an SDRAM is defined by the
18 logic state of the control signals at a particular point in time—that is, the bits (0s or 1s)
19 represented by those control signals at that time—and the command is recognized only as a result
20 of a transition of the clock signal from low to high (a rising edge of the clock signal).

21 **B. Rambus's Inventions**

22 In the late 1980s, computer central processing units (CPUs) were increasing in
23 performance at a rate that would soon outpace the capabilities of the then state-of-the-art memory
24 systems. A memory system that could not provide data to a CPU as fast as that CPU was ready
25 for it would slow down the effective speed of the CPU—the CPU would have no choice but to
26 wait for the data from the memory. This problem was referred to as the “memory bottleneck.”

27 Electrical engineering professors Michael Farmwald and Mark Horowitz, the two
28 founders of Rambus and the named inventors on the patents-in-suit recognized that the stop-gap

1 solution, adding more memory devices operating in parallel to supply the CPU with data, was not
 2 sustainable. To solve the memory bottleneck problem, Farmwald and Horowitz devised a
 3 comprehensive solution that was comprised of multiple individual inventions. On April 18, 1990,
 4 Rambus filed patent application serial no. 07/510,898 which disclosed numerous inventions and
 5 claimed eleven distinct groups of inventions, as made clear by the 11-way restriction requirement
 6 imposed by the Patent Examiner in his initial action on the case. Rambus elected one group of
 7 inventions to continue prosecuting in the '898 application and, on March 6, 1992, filed ten
 8 divisional applications to pursue the other groups. Since then, Rambus has filed numerous other
 9 continuation and divisional applications claiming priority to the original '898 application,
 10 including the applications that resulted in the nine patents currently at issue in this case. (All told,
 11 Rambus has been issued over 50 patents that claim priority to the '898 application).

12 Though the speed and efficiency of a memory system is most dramatically improved
 13 through use of all of Farmwald and Horowitz's claimed inventions, the inventions may be used
 14 individually, or in a combination of less than all to achieve more modest speed and efficiency
 15 gains. Indeed, LSI's and STMicro's accused devices incorporate only some of Rambus's
 16 inventions, including those claimed by the asserted claims in this case. Many of the asserted
 17 patent claims in this case contain limitations directed to one or more of the following features that
 18 are illustrative examples of Rambus's speed and efficiency enhancing inventions.

19 1. Programmable Latency

20 Some of the asserted claims (for example, claim 23 of the U.S. Patent No. 6,038,195⁵)
 21 involve the controller sending a value representative of a delay time, or latency, for storage in a

22 ⁵ Claim 23 of the '195 patent claims:

23 23. A method of controlling a synchronous memory device having at least one memory
 24 section including a plurality of memory cells and a register for storing a value which is
 25 representative of a time delay after which the memory device responds to a read request,
 the method comprising:

26 issuing a read request to the memory device; and

27 receiving data from the memory device, in response to the read request, wherein the
 28 memory device outputs the data after the time delay transpires and synchronously with
 respect to an external clock signal.

1 register on a synchronous memory device, such as an SDRAM. This delay time causes the
 2 memory device to wait until after the delay time has elapsed to respond to a read command. At
 3 first blush, it may seem counterintuitive that the insertion of a delay time would improve the
 4 speed and efficiency of the system, and, in fact, at the time, the industry was focused on
 5 *decreasing* DRAM latency. As discussed above, for example, asynchronous DRAMs output data
 6 onto the data lines as soon as data was read from the memory array into the sense amplifiers. In
 7 contrast, Farmwald and Horowitz taught that insertion of a known/controlled delay time can
 8 improve memory system performance. Much like the way in which traffic lights slow down
 9 individual cars but improve overall traffic flow, proper use of delay times improves the overall
 10 performance of the interface between the processor and the memory device. Rambus's invention
 11 is not simply the imposition of a delay time; rather it is the implementation of the delay time as a
 12 programmable value (sent by the controller for storage in a register). The controller could then
 13 use the invention to optimize the delays for the system in which it is being used.

14 SDRAM and DDR SDRAM memory systems allow for programming the read latency, as
 15 described above, but not the write latency. That is the delay time between when the controller
 16 sends a write command and when it sends the corresponding data to be input by the DRAM was
 17 fixed and could not be adjusted. Beginning with DDR2 memory systems, however, functionality
 18 was added to allow write latency to be programmed as well.

19 2. Variable Block Size

20 Another of Rambus's inventions (see, for example, claim 1 of U.S. Patent No. 6,034,918⁶)

21 ⁶ Claim 1 of the '918 patent claims:

22 1. A method of controlling a synchronous memory device, wherein the memory device
 23 includes a plurality of memory cells, the method of controlling the memory device
 comprises:

24 providing first block size information to the memory device, wherein the first block size
 25 information defines a first amount of data to be output by the memory device onto a bus in
 response to a read request; and

26 issuing a first read request to the memory device, wherein in response to the first read
 27 request, the memory device outputs the first amount of data corresponding to the first
 28 block size information onto the bus synchronously with respect to an external clock
 signal.

(continued...)

1 involves the controller sending “block size information” to a synchronous memory device so that
 2 the device can return a variable amount of data depending on the value of the block size
 3 information in a read operation (or input a variable amount of data in a write operation). Thus,
 4 rather than returning a single bit of data per output pin to the controller in response to a read
 5 command, the memory device could respond with, say, four bits or eight bits or other amounts of
 6 data. The controller could then set the amount of data to a value that optimizes the performance
 7 of the system or application.

8 3. Dual-Edge Clocking

9 A number of the asserted claims (for example, claim 33 of the U.S. Patent No. 6,584,037⁷)
 10 provide for data to be input or output with reference to both rising and falling edges of the clock
 11 signal, as opposed to just one edge, thereby allowing two bits of data to be transferred on each
 12 data line per clock cycle. While SDRAM memory systems allow for data transfer only on rising
 13 edges of the clock signal, DDR SDRAM memory systems, as the inclusion of “double data rate”
 14 in the name suggests, began providing for the transfer of data synchronously with respect to both
 15 the rising and falling edges of the clock signal.

16 4. Auto Precharge

17 Another of Rambus’s inventions (see, for example, claim 27 of the ’037 patent⁸) provides

18 (...continued)

19 ⁷ Claim 33 of the ’037 patent is a dependent claim that adds dual-edge clocking related
 20 limitations:

21 33. The method of claim 25 wherein outputting the data to the memory
 device includes:

22 outputting a first portion of the data synchronously with respect to a rising
 23 edge transition of the clock signal; and

24 outputting a second portion of the data synchronously with respect to a
 falling edge transition of the clock signal.

25 ⁸ Claim 27 of the ’037 patent is a dependent claim that adds auto precharge related limitations:

26 27. The method of claim 25 wherein the first operation code includes
 27 precharge information that specifies that the memory device precharge a
 plurality of sense amplifiers after the write operation, wherein the plurality
 28 of sense amplifiers is used in writing the data to the plurality of memory

(continued...)

1 for the controller to send precharge information to a synchronous memory device together with a
 2 read or write command. The sense amplifiers on a DRAM must be precharged—that is brought
 3 to voltage mid-way between high and low voltages—before a new row is activated. *See* note 3,
 4 *supra*. Sending precharge information with the read or write command, improves system
 5 efficiency because it obviates the need for the controller to send a separate precharge command.

6 **III. LEGAL PRINCIPLES**

7 While there is “no magic formula” by which a court should construe patent claims, “[t]he
 8 construction that stays true to the claim language and most naturally aligns with the patent’s
 9 description of the invention will be, in the end, the correct construction.” *Phillips v. AWH Corp.*,
 10 415 F.3d 1303, 1316, 1324 (Fed. Cir. 2005). The primary determinants of the meaning of a term
 11 are the intrinsic evidence, *i.e.*, the claim language, the specification, and the prosecution history.

12 Construction begins with the language of the claim, and claim terms should be given their
 13 ordinary and customary meaning, *Callicrate v. Wadsworth Mfg., Inc.*, 427 F.3d 1361, 1366-67
 14 (Fed. Cir. 2005), with the ordinary and customary meaning referring to how “a person of ordinary
 15 skill in the art in question” would understand a claim term “at the time of the invention, *i.e.*, as of
 16 the effective filing date of the patent application.” *Phillips*, 415 F.3d at 1313. “Such a person is
 17 deemed to read the claim term in the context of the entire patent, including the other claims and
 18 the written description.” *Biagro W. Sales, Inc. v. Grow More, Inc.*, 423 F.3d 1296, 1302 (Fed.
 19 Cir. 2005). The written description thus plays a “key role” in the interpretation of the claims.
 20 *nCube Corp. v. Seachange Int’l, Inc.*, 436 F.3d 1317, 1327 (Fed. Cir. 2006); *Vitronics Corp. v.*
 21 *Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996) (specification is “highly relevant to the
 22 claim construction analysis,” usually “dispositive,” and “the single best guide to the meaning of a
 23 disputed term”). There need be no express definition of a claim term in the specification; rather,
 24 “the specification may define claim terms by implication such that the meaning may be found in
 25 or ascertained by a reading of the patent documents.” *Phillips*, 415 F.3d at 1321 (quoting *Irdeto*
 26 *Access, Inc. v. Echostar Satellite Corp.*, 383 F.3d 1295, 1300 (Fed. Cir. 2004)).

27 (...continued)
 28 cells during the write operation.

Another source of intrinsic evidence is the prosecution history, which “demonstrat[es] how the inventor understood the invention and whether the inventor limited the invention in the course of prosecution, making the claim scope narrower than it would otherwise be.” *Phillips*, 415 F.3d at 1317. However, such claim narrowing is appropriate only where the prosecution history contains “a sufficiently clear and deliberate statement to meet the high standard for finding a disclaimer of claim scope.” *Honeywell Int’l, Inc. v. Universal Avionics Sys. Corp.*, 493 F.3d 1358, 1365 (Fed. Cir. 2007).

The final interpretative source is evidence extrinsic to the patent, that is, “all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.” *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 980 (Fed. Cir. 1995). In particular, “[b]ecause dictionaries, and especially technical dictionaries, endeavor to collect the accepted meanings of terms used in various fields of science and technology, those resources have been properly recognized as among the many tools that can assist the court in determining the meaning of particular terminology to those of skill in the art of the invention.” *Phillips*, 415 F.3d at 1318. However, extrinsic evidence may not “be used to change the meaning of claims in derogation of the [intrinsic evidence]” and should be “considered in the context of the intrinsic evidence.” *Id.* at 1319.

In addition, Judge Whyte has previously construed many of the claim terms at issue in *Hynix I*⁹ and the *Coordinated Actions*,¹⁰ litigation also involving patents from the Farmwald/Horowitz family and including some of the same patents in suit as in this case. The Supreme Court has stressed “the importance of uniformity in the treatment of a given patent.” *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 390 (1996). Thus, while Judge Whyte’s prior constructions do not constitute binding authority, “to the extent that the [prior claim construction order] addresses identical or similar issues of claims construction, it can be viewed

⁹ *Hynix Semiconductor Inc. et al. v. Rambus Inc.*, No. 00-cv-20905-RMW (N.D. Cal.).

¹⁰ *Rambus Inc. v. Hynix Semiconductor Inc., et al.*, No. 05-cv-00334-RMW (N.D. Cal.); *Rambus Inc. v. Samsung Electronics Co. Ltd., et al.*, No. 05-cv-02298-RMW (N.D. Cal.); and *Rambus Inc. v. Micron Technology, Inc., et al.*, No. 06-cv-00244-RMW (N.D. Cal.).

as persuasive and highly relevant.” *Verizon Cal. Inc. v. Ronald A. Katz Tech. Licensing, P.A.*, 326 F. Supp. 2d 1060, 1069 (C.D. Cal. 2003); *see also Comcast Cable Commc’ns. Corp. v. Finisar Corp.*, 2007 WL 1052821, at *2 (N.D. Cal. Apr. 6, 2007) (although prior district court constructions are not binding, “there is an interest in *stare decisis* and uniformity in the treatment of the same patent”).

Likewise, the fact that Rambus’s prior litigation opponents agreed to certain of the constructions that Rambus proposes here is a relevant fact that the Court should take into consideration. *See Civix-DDI, LLC v. Hotels.Com, L.P.*, 2010 WL 4386475, at *9 (N.D. Ill. Oct. 25, 2010) (holding prior agreed construction involving different parties relevant though not controlling). Such agreed constructions are especially relevant in this case given that the prior litigation opponents in question are sophisticated technology companies unlikely to agree to incorrect constructions of the terms at issue.

IV. SPECIFIC CLAIM TERMS

A. “controller”/“controller device”

The parties agree that the terms “controller” and “controller device” should each receive the same construction.¹¹ However, while Rambus proposes that the terms be construed as “an integrated circuit device that includes circuitry to direct the actions of one or more memory devices,” Defendants propose “a device that controls one or more devices.”

As an initial matter, Defendants’ proposed definition is circular, as it defines “controller” in terms of the word “controls.” Moreover, Defendants’ definition is pitched at such a high level of generality as to render it completely divorced from the context of the claims and the patent specification, contrary to the claim construction guidelines discussed above that stress the importance of the claims and the specification in claim construction. The claims establish on their face that the controller/controller device is not a generic controller but one directed to controlling a memory device. For example, claim 15 of the ’916 patent recites “a method of

¹¹ The asserted claims in which the various terms at issue appear are set forth in Appendix A to the Joint Claim Construction and Prehearing Statement, *LSI Dkt. #95-1*.

controlling a synchronous memory device by a controller,” and claim 18 of U.S. Patent No. 6,304,937 patent recites “[a] controller device for controlling a synchronous memory device[.]” A consideration of the terms within the context of the claims thus makes it evident that Defendants’ proposed definition is inappropriate.

Additionally, the specification makes clear that a “controller device” is a type of integrated circuit device and that it controls, that is directs the actions of, one or more memory devices, as Rambus’s proposed construction provides. Indeed, the specification opens by describing the “Field of the Invention” as follows: “An *integrated circuit* bus interface for computer and video systems is described which allows high speed transfer of blocks of data, particularly to and from memory devices, with reduced power consumption and increased system reliability.” ’916 patent, col. 1:22-27 (emphasis added). The specification goes on to make clear that this novel bus interface is “built into semiconductor devices.” *Id.*, col. 3:24-25. These semiconductor devices may be controller devices or memory devices. *Id.*, col. 6:16-21 (“The bus architecture of this invention connects master or bus *controller devices*, such as CPUs, Direct Memory Access devices (DMAs) or Floating Point Units (FPUs), and slave devices, such as DRAM, SRAM or ROM memory devices.”) (emphasis added). In light of the technology described in the specification, it is appropriate to construe “controller” and “controller device” as integrated circuit devices that control—i.e., direct the actions—of memory devices.

By contrast, Defendants’ proposed construction is wholly unmoored from the context of the claims and specification—it encompasses the sorts of controller devices described in the Farmwald/Horowitz patents as well as, potentially, the anti-lock brake controller on an automobile, the controller of a backyard irrigation system, and a host of other technologies with no connection whatsoever to the patented inventions at issue here.

It is instructive that Hynix, one of Rambus’s litigation opponents, has agreed that, for purposes of the Farmwald/Horowitz patents, “memory controller” means “[a]n integrated circuit device that includes circuitry to direct the actions of one or more memory devices,” Detre Decl., Ex. B (*Hynix I* Joint Claim Construction and Prehearing Statement (hereinafter “*Hynix I* JCCS”)), at 2, just as Rambus has proposed for controller/controller device here. The claims and the

specification, discussed above, make clear that, the “controllers” in the asserted claims are, in fact, “memory controllers,” and should be construed the same way.

B. “clock signal”/“external clock signal”

Rambus proposes that “clock signal” be construed as “a periodic signal, i.e., one that is continuously present and repeats at regular intervals, to provide timing information.” Defendants propose that the term be construed as “a periodic signal that is continuously present and repeats at regular intervals to provide timing information.”¹² Thus, the dispute focuses on whether a periodic signal *necessarily* is continuously present and repeats at regular intervals, as Rambus asserts, or whether those are simply features of the particular periodic signals at issue here, as Defendants’ proposed construction suggests.

It is well understood that a periodic signal is one that repeats at regular intervals. *See, e.g.,* Detre Decl., Ex. H (Webster’s New World Dictionary of American English, 3d College Ed. (1988) (hereinafter “1988 Webster’s Dictionary”)), at 1004 (definition 1 of “periodic”: “occurring, appearing, or recurring at regular intervals”). Thus while it may be appropriate to point out that a periodic signal repeats at regular intervals, as per Rambus’s construction, Defendants’ construction that suggests that this is simply a property of the particular periodic signals at issue here (but not other periodic signals) is incorrect. Moreover, a signal that was not continuously present obviously could not repeat at regular intervals, because any pattern would be interrupted during the times when the signal was not present. Thus, the construction should make clear that the continuous presence of the periodic signal is part of what it means to be periodic.

Judge Whyte has construed “external clock signal” as “[a] periodic signal from a source external to the device to provide timing information,” Detre Decl., Ex. E (*Coordinated Actions* Claim Construction Order for the Farmwald/Horowitz Patents (hereinafter “*Coordinated Actions* CC Order”)), at 50, and saw no need to put any further gloss on the meaning of “periodic.”

¹² There is no additional dispute regarding “external clock signal.” The parties’ proposed constructions both recognize that the construction of “external clock signal” should be the construction of “clock signal,” modified by adding the clause “from a source external to the device.” Joint Claim Construction and Prehearing Statement, Appendix A, *LSI* Dkt. # 95-1, at 2.

Rambus originally proposed Judge Whyte's construction here, but, as a compromise, agreed to make clear in the construction that a periodic signal was continuously present and repeated at regular intervals. Defendants' proposed construction which improperly suggests that these are not necessary features of periodic signals should be rejected.

C. "operation code"

Rambus has proposed that "operation code" be construed as "one or more bits to specify a type of action," while Defendants propose "one or more control bits to specify a type of action." Thus, Defendants' proposed construction is identical to Rambus's, except that Defendants specify that the "bits" at issue are "*control* bits."

Defendants' proposed construction injects potential uncertainty and confusion into the straightforward definition of "operation code." The specification makes clear that information specifying a type of action *is* control information. *See, e.g.*, '916 patent, col. 9:45-49, 54-57 (indicating that "control information" includes AccessType field, specifying, for example, whether the requested operation is a read or write). Thus, the concept of "control" is captured in the provision that the bits "specify a type of action," which is contained in both sides' proposed constructions of "operation code." This understanding of "control" is also consistent with Rambus's proposed definition of "controller," discussed above, as "an integrated circuit device that includes circuitry to *direct the actions* of one or more memory devices." To the extent that all Defendants mean by "control bits" is that the bits specify a type of action, their proposed construction is redundant, and consequently confusing because it would suggest that "control" is intended to convey something more than specifying an action. To the extent that Defendants do mean something else by "control bits," it is unclear what that meaning would be—the term "control bits" appears nowhere in the specification and is not a commonly understood term of art—and would likewise cause confusion.

Rambus's construction follows Judge Whyte's construction in prior litigation over the Farmwald/Horowitz patents. Detre Decl., Ex. E (*Coordinated Actions* CC Order), at 37-39; Detre Decl., Ex. C (*Hynix I* Claim Construction Order (hereinafter "*Hynix I* CC Order")), at 14-19. There is no reason to deviate from that construction here.

1 **D. “precharge information”**

2 Rambus has proposed that “precharge information” be construed as “one or more bits
3 indicating whether the sense amplifiers and/or bit lines (or a portion of the sense amplifiers and/or
4 bit lines) should be precharged.” Defendants’ assert, in the first instance that the term should
5 simply be given its ordinary, plain meaning and that, consequently, no construction is required.
6 Alternatively, Defendants propose a construction that is identical to Rambus’s, except that they
7 have replaced “one or more bits indicating” with “information denoting.”

8 As an initial matter, the Court should construe “precharge information” because
9 Defendants’ alternative proposed construction of the term indicates that there is a dispute between
10 the parties. *See O2 Micro Int’l Ltd. v. Beyond Innovation Tech. Co.*, 521 F.3d 1351, 1361 (Fed.
11 Cir. 2008) (“A determination that a claim term ‘needs no construction’ or has the ‘plain and
12 ordinary meaning’ may be inadequate when a term has more than one ‘ordinary’ meaning or
13 when reliance on a term’s ‘ordinary’ meaning does not resolve the parties’ dispute.”)

14 Defendants’ proposed construction is not necessarily incorrect, but its definition of
15 “information” as “information” is circular and ambiguous. In the context of the patent
16 specification, the “information” at issue consists of “one or more bits” and the construction
17 should so indicate. Every reference to control information—such as the precharge information at
18 issue here—in the specification makes clear that this information consists of some number of bits.
19 For example, the specification indicates that, in the preferred embodiment, control information is
20 sent to the memory devices in “two 4 *bit* fields.” ’916 patent, col. 9:46-47 (emphasis added).
21 The specification further indicates that “precharge information” is included in the bits of control
22 information. After noting that one of the 4-bit fields of control information is an “AccessType”
23 field, the specification describes how this field “provides for access mode control specifically for
24 the DRAMs” and, in particular, determines whether the DRAM should precharge the sense
25 amplifiers or should save the contents of the sense amps for a subsequent page mode access.” *Id.*,
26 col. 10:22-23, 47-50. One particular bit of the AccessType field is specified to be the
27 “precharge/save-data switch.” *Id.*, col. 11:44.

1 Rambus’s proposed construction is also consistent with the Federal Circuit’s prior
 2 construction of terms from the Farmwald/Horowitz patents. Specifically, in *Rambus Inc. v.*
 3 *Infineon Techs. Ag*, 318 F.3d 1081, 1093 (Fed. Cir. 2003), the court construed “read request” as
 4 “a series of *bits* used to request a read of data from a memory device where the request identifies
 5 what type of read to perform,” and “write request” as “a series of *bits* used to request a write of
 6 data to a memory device.” (Emphasis added.) The parties have agreed that these constructions
 7 are controlling here. Joint Claim Construction and Prehearing Statement (hereinafter, “JCCS”),
 8 *LSI Dkt. # 95*, at 1. A read request is, of course, an example of control information sent to the
 9 memory device—in this case, control information requesting that the memory device output data
 10 stored in it. Thus, the Federal Circuit deemed it appropriate to specify that control information
 11 sent to the memory devices in the claims of the Farmwald/Horowitz consisted of “bits.”

12 Finally, Rambus’s construction follows Judge Whyte’s construction in the Coordinated
 13 Actions. Detre Decl., Ex. E (*Coordinated Actions* CC Order) at 88. While Judge Whyte initially
 14 construed “precharge information” consistently with Defendants’ alternative construction, Detre
 15 Decl., Ex. C (*Hynix I* CC Order), at 21-23, he subsequently deemed it appropriate to specify that
 16 the “information” at issue consisted of “one or more bits” in his most recent construction of the
 17 term. The Court should do likewise here.

18 **E. “register”**

19 Rambus proposes that “register” be construed as “a data storage element or group of data
 20 storage elements not part of a memory array that can store one or more bits of information.”
 21 Defendants’ proposal—“a storage element that can store information”—is contrary to the patent
 22 specification and the understanding of those of skill in the art.

23 Defendants’ proposed construction departs from the proper construction of the term in a
 24 number of ways. Most significantly, Defendants’ proposed construction is so broad that it would
 25 allow a register to be a memory cell in the memory array contrary to the ordinary meaning of the
 26 term and the patent specification. The specification consistently refers to registers as storage
 27 elements that store information separate from the data stored in the memory array. For example,
 28 the specification notes that “[r]egisters are provided which may store control information, device

1 identification, device-type and other information appropriate for the chip such as the address
 2 range for each independent portion of the device.” ’916 patent, col. 4:23-27. As another
 3 example, the specification notes that “each semiconductor device contains a set of internal
 4 registers 170, preferably including a device identification (device ID) register 171, a device-type
 5 descriptor register 174 control registers 175 and other registers containing other information
 6 relevant to that type of device.” ’916 patent, col. 6:31-37. Indeed, the title of the ’916 patent—
 7 “Memory device having a variable data output length and a programmable *register*”—would
 8 make no sense if a register could consist of a memory cell in the memory array because, in that
 9 case, every memory device would automatically contain a multitude of programmable registers.

10 By contrast, and consistent with ordinary usage, the specification uses the term “memory
 11 cells,” not “register,” to refer to storage elements in the memory array. *See, e.g.*, ’916 patent, col.
 12 23:53-54 (“Each subarray is divided into arrays 148, 149 of memory cells.”); *accord* Detre Decl.,
 13 Ex. G (IEEE Standard Dictionary of Electrical and Electronics Terms, 5th Ed. (1993) (hereinafter
 14 “1993 IEEE Dictionary”)), at 797 (defining “memory cell” as “[t]he smallest subdivision of a
 15 memory into which a unit of data has been or can be entered . . .”).

16 In addition, the specification makes clear that a register must store bits of information, as
 17 Rambus’s proposed construction provides. For example, the specification notes information to be
 18 stored in a control register may be included in certain “bytes” transmitted by the controller to a
 19 memory device. ’916 patent, col. 10:13-15. A byte is eight bits. Detre Decl., Ex. F (IEEE
 20 Standard Dictionary of Electrical and Electronics Terms, 4th Ed. (1988) (hereinafter “1988 IEEE
 21 Dictionary”)), at 118 (definition (1) of “byte”: “A binary bit string operated on as a unit and
 22 usually eight bits long . . .”).

23 The specification also establishes that a register need not consist of a single storage
 24 element, which suggests that it could store only a single bit of information, as Defendants’
 25 proposed construction incorrectly provides. For example, the specification states that “[i]n the
 26 preferred embodiment, each device connected to the bus contains a special device-type register
 27 which specifies the type of device, for instance CPU, 4 MBit memory, 64 MBit memory or disk
 28 controller.” ’916 patent, col. 14:64-67. Even if there were only four possible types of devices,

1 and the specification implies that the four types listed are just examples, a single bit, which can
 2 only represent two values, would not suffice to distinguish them. Therefore, the Court should
 3 adopt Rambus's proposed construction, including that a register can consist of "a data storage
 4 element or group of data storage elements."

5 Several of Rambus's prior litigation opponents including Hynix, Micron, and Samsung
 6 and Nanya have agreed with Rambus's proposed construction here, strongly suggesting that this
 7 is the appropriate construction of the term. Detre Decl., Ex. D (*Coordinated Actions* Joint Claim
 8 Construction and Prehearing Statement (hereinafter, "*Coordinated Actions* JCCS")), at 3; Detre
 9 Decl. Ex. B (*Hynix I* JCCS), at 2. The Court should, therefore, adopt Rambus's proposed
 10 construction.

11 **F. "representative of"**

12 Rambus proposes that "is representative of" be construed as "indicates," while Defendants
 13 assert that the term should be given its ordinary, plain meaning and that no construction is
 14 required. The term appears in phrases such as "the value is representative of a number of cycles
 15 of an external clock signal to transpire" and "the block size information is representative of an
 16 amount of data to be output by the memory device," '916 patent, claim 15, as well as other
 17 similar phrases.

18 Absent a construction of the term, Rambus is concerned that Defendants could try to argue
 19 that any relationship between two values means that one is "representative of" the other. This
 20 concern is not purely theoretical. Rambus's prior litigation opponents in the *Coordinated Actions*
 21 sought to read "representative of" very broadly in order to argue that certain Rambus patent
 22 claims were anticipated by prior art. Judge Whyte, however, rejected such a broad reading of the
 23 term:

24 [O]ne value being "representative" of another requires more than a
 25 functional relationship between the two. The word "representative"
 26 implies some level of recognition by another that the first value
 27 *indicates* or represents the second. The verb "represent" means
 28 "[t]o bring clearly and distinctly before the mind, esp. (to another)
 by description" and "[t]o symbolize, to serve as a visible or
 concrete embodiment of (some quality, fact, or other abstract
 concept)." Oxford English Dictionary (2d ed. 1989) (definitions 2a
 and 6a).

Order Denying Motion for Summary Judgment No. 1 of Invalidity, 05-cv-00334-RMW, Dkt. No. 2873, at 24 (emphasis added). *Accord* Detre Decl., Ex. H (1988 Webster’s Dictionary), at 1139 (definitions 1 and 4a for “represent”: “to present or picture to the mind,” “to be a sign or symbol for; stand for; symbolize”). The Federal Circuit has likewise concluded that “the statement that one item ‘represents’ another cannot be interpreted so broadly as to include any case in which the two items are related in some way.” *Tehrani v. Hamilton Med., Inc.*, 331 F.3d 1355, 1361 (Fed. Cir. 2003).

Construing “is representative of” as “indicates” is consistent with the caselaw and dictionary definitions cited above and would make clear that for one value to be representative of another there must be more than simply some relationship between the values. Moreover, Rambus’s proposed construction is consistent with Judge Whyte’s prior construction of various phrases that included the term. *See* Detre Decl., Ex. C (*Hynix I* CC Order), at 28 (replacing “is representative of” with “indicates” in construction of certain phrases, such as “value that is representative of an amount of time to transpire”). Because “reliance on . . . ‘ordinary’ meaning does not resolve the parties’ dispute” regarding the meaning of “representative of,” *O2 Micro*, 521 F.3d at 1361, Rambus requests that the Court construe the term and adopt Rambus’s proposed construction.

G. “sample(s)”/“sampled”/“sampling”

Rambus submits that to “sample” should be construed as to “obtain at one or more discrete points in time.” Defendants assert that to “sample” simply means to “capture.”

Defendants’ position finds no support in the intrinsic evidence or in the ordinary meaning of the term. Just as in ordinary parlance to “sample” something means to take only part of it, in reference to an electronic signal, to “sample” means to obtain only some of the values of the signal—namely, the values of the signal at discrete points in time. *See* Detre Decl., Ex. F (1988 IEEE Dictionary), at 855 (defining “sampled data” as “[d]ata in which the information content can be, or is, ascertained only at discrete intervals of time”). Thus, while “sampling” does involve capturing values of a signal, it is well understood in the art to refer to capturing those values only at discrete points in time, rather than, for example, continuously. Defendants’

1 proposed construction fails to convey this critical distinction between “sampling” and
 2 “capturing.” Indeed, because according to Defendants’ proposed construction to “sample” a
 3 signal means to “capture” *the signal*, Defendants’ construction incorrectly implies that sampling a
 4 signal involves capturing the entire signal.

5 The specification of the patents-in-suit uses the term in its ordinary sense, with
 6 “sampling” referring to obtaining the values of a signal at discrete time intervals, at the transitions
 7 of a clock signal. For example, the specification refers to “clocked receivers”—that is, receivers
 8 that obtain values when a clock signal transitions—that “sample” input signals, ’916 patent, col.
 9 21:61-62. Elsewhere, the specification notes that “input receivers 101 and 111 sample the bus
 10 clocks just as they transition,” *id.* col. 23:12-14, making clear that the receivers obtain the values
 11 of the bus clocks at the discrete transition times. The specification also refers to the “sample
 12 period”—namely, the interval between successive sampling of the signal—which would make no
 13 sense if “sampling” referred to continuously capturing the value of the signal. *Id.*, col. 22:45.

14 Here, again, Rambus is following Judge Whyte’s construction of “sample.”¹³ Detre
 15 Decl., Ex. E (*Coordinated Actions* CC Order), at 53-55. Defendants, on the other hand, have
 16 proposed a definition counter to Judge Whyte’s construction, the patent specification, and
 17 ordinary meaning. The Court should adopt Rambus’s proposed construction.

18 **H. “synchronous dynamic random access memory device”**

19 Rambus proposes that “synchronous dynamic random access memory device”—i.e.,
 20 “synchronous DRAM device”—be construed as “an integrated circuit device in which
 21 information can be stored and retrieved electronically, not including a memory controller, that
 22 _____

23 ¹³ Rambus’s proposed construction is a minor adjustment of Judge Whyte’s. Judge Whyte had
 24 construed “sample” to mean “to obtain a discrete point in time,” and “samples” to mean “obtains
 25 at discrete points in time.” Detre Decl., Ex. E (*Coordinated Actions* CC Order), at 55. But the
 26 claims use “sample(s)” as a verb, and whether an “s” appears on the end relates simply to the
 27 conjugation of the verb and not to the number of points sampled as Judge Whyte’s construction
 28 may suggest. *Compare, e.g.*, U.S. Patent No. 6,304,937, claim 18 (including limitation “input
 receiver circuitry to sample the first portion of data”), *with id.*, claim 23 (including limitation “the
 input receiver circuitry samples an amount of data”). It is, therefore, more appropriate to construe
 both “sample” and “samples” as referring to obtaining at one or more discrete points in time, as in
 Rambus’s proposed construction.

1 receives an external clock signal which governs the timing of the response to a read request, write
 2 request, or operation code and includes one or more arrays of DRAM cells.” Defendants, on the
 3 other hand, propose that the term should be construed as “a dynamic random access memory
 4 device in which an external clock signal is used to regulate the timing of device operations.”

5 The parties have agreed that the Federal Circuit’s construction of “integrated circuit
 6 device” as “a circuit constructed on a single monolithic substrate, commonly called a ‘chip’”
 7 should control here. JCCS, *LSI* Dkt. # 95, at 1. With respect to the construction of “synchronous
 8 DRAM device,” the principal disputes between the parties are (1) whether a “synchronous
 9 DRAM device” is such an integrated circuit device, i.e., whether it is a single chip, (2) whether a
 10 synchronous DRAM device may include a memory controller, and (3) what the requirement that
 11 the device be “synchronous” entails.¹⁴

12 With respect to the first dispute, a review of the patent specification confirms that DRAM
 13 is used in the ordinary sense to refer to a single dynamic random access memory chip. *See, e.g.,*
 14 ’916 patent, col. 3:43-45 (referring to “DRAM chips”). Numerous figures also illustrate DRAM
 15 chips. ’916 patent, Figs. 1, 2, 3, 9, 15 and associated text at cols. 1:61-64, 3:63-66, 4:22-49, 21:1-
 16 5, 23:51-52. Moreover, there can be no argument that a “DRAM” is a single chip, but a “DRAM
 17 device” is not: the specification uses the two terms interchangeably. *See, e.g.,* ’916 patent, col.
 18 4:22-28 (referring to DRAMs as “DRAM devices”); col. 16:40 (same). Thus, there is no question
 19 that a DRAM device, and in particular a synchronous DRAM device, is a single chip.

20 Rambus expects Defendants to argue, as a number of Rambus’s prior litigation opponents
 21 have argued, that a “memory device” is not limited to a single chip and, so, is not necessarily an
 22 integrated circuit device.¹⁵ Any such argument would be beside the point, however, because,

23 ¹⁴ In addition, Defendants’ proposed construction is circular because it defines “synchronous
 24 dynamic random access memory device” in terms of a “dynamic random access memory device.”

25 ¹⁵ The question of whether a “memory device,” as the term is used in the Farmwald/Horowitz
 26 patents, is an integrated circuit device is currently before the Federal Circuit. In connection with
 27 the reexamination of U.S. Patent No. 6,034,918, one of the patents in suit here, the Board of
 28 Patent Appeals and Interferences (BPAI) ruled that a memory device is not necessarily limited to
 a single chip (i.e., is not necessarily an integrated circuit device). Rambus appealed that ruling to
 the Federal Circuit and the appeal was argued on February 7, 2012. A decision as to the

(continued...)

1 regardless of whether a “memory device” refers to a single chip in the Farmwald/Horowitz
 2 patents (and Rambus maintains that it does), as discussed above, the specification makes clear
 3 that a *synchronous dynamic random access* memory device does refer to a single chip. Indeed,
 4 even though he found that a “memory device” was not necessarily limited to a single chip, Judge
 5 Whyte agreed that a “synchronous dynamic random access memory device” was so limited. *See*
 6 Detre Decl., Ex. E (*Coordinated Actions CC Order*), at 35 (“These additional limits on the scope
 7 of ‘memory device’ . . . demonstrat[e] that Rambus knew how to limit its claims to a single chip
 8 when it wished to do so.”). Likewise, although the BPAI ruled that a “memory device” was not
 9 limited to a single chip in the decision currently on appeal to the Federal Circuit, *see* note 15,
 10 *supra*, it indicated that a “memory (DRAM) device” would be considered a single chip. *See*
 11 Detre Decl., Ex. I (BPAI Decision on Appeal, Appeal 2010-011178), at 29 (finding based on
 12 claim differentiation that “memory device” in certain claims should be construed more broadly
 13 than a single chip in light of other claim drawn “more narrowly to a ‘memory (DRAM) device’”).

14 With respect to the second dispute, Rambus maintains that a synchronous DRAM device
 15 cannot include a memory controller. The term “master” is used in the specification to refer to a
 16 controller, while the term “slave” refers to a device being controlled. *See* ’916 patent, col. 6:16-
 17 20. The specification makes clear that “a memory device will typically have only slave
 18 functions,” that is, it will not include a controller. *See, e.g., id.*, col. 6:24-26. The Federal
 19 Circuit’s ruling on the appropriate construction of “memory device” is expected to determine
 20 whether a memory device, and therefore a synchronous dynamic random access memory device,
 21 may or may not include a memory controller, and will be binding here. *See Key Pharms. v.*
 22 *Hercon Labs. Corp.*, 161 F.3d 709, 716 (Fed. Cir. 1998) (recognizing “the national *stare decisis*
 23 effect that this court’s decisions on claim construction have”).

24 Finally as to the third dispute, Rambus’s proposed construction provides that, for a
 25 memory device to be “synchronous,” it must “receive[] an external clock signal which governs
 26 the timing of the response to a read request, write request, or operation code,” while Defendants

27 (...continued)
 28 appropriate construction of “memory device” is, consequently, expected shortly.

1 propose that an external clock signal be “used to regulate the timing of device operations.” Both
 2 sides agree that a “synchronous” memory device must use an external clock signal for timing
 3 purposes, but Defendants’ proposed definition is vague and leaves open questions such as
 4 whether all device operations must be “regulate[d]” by the external clock signal or only certain
 5 ones (and, if the latter, which ones). The specification, however, makes clear that the external
 6 clock signal governs timing with respect to signals that travel on the bus connecting the memory
 7 controller to the memory devices. *See, e.g.*, ’916 patent, col. 8:35-47 (describing clocking
 8 scheme, using “synchronized, high speed clock for all devices on the bus” that governs bus cycles
 9 for transmitting signals on the bus). Thus, the external clock, as provided in Rambus’s proposed
 10 construction, governs the memory device’s response to commands from the memory controller,
 11 namely read and write requests (or operation codes specifying a read or write operation).

12 Similar to Rambus’s proposed construction here, Judge Whyte has construed
 13 “synchronous memory device” for purposes of the Farmwald/Horowitz patents as “a memory
 14 device that receives an external clock signal which governs the timing of the response to a
 15 transaction request.” Detre Decl., Ex. C (*Hynix I CC Order*), at 11-14; Detre Decl., Ex. E
 16 (*Coordinated Actions CC Order*), at 53. Here none of the claims at issue include the term
 17 “transaction request,” so Rambus has adjusted Judge Whyte’s construction by replacing
 18 “transaction request” with the types of commands that the controller issues and that the memory
 19 devices respond to in the asserted claims: a read request, a write request, or an operation code
 20 (specifying a read or write instruction). *See, e.g.*, U.S. Patent No. 6,034,918, claim 1 (involving
 21 response of memory device to “first read request”); U.S. Patent No. 6,260,097, claim 1 (involving
 22 response of memory device to “write request”); ’916 patent, claim 15 (involving response of
 23 memory device to “first operation code”). The Court should follow Judge Whyte’s reasoning and
 24 adopt Rambus’s proposed construction here.

25 **I. “synchronously with respect to”**

26 Rambus proposes that “synchronously with respect to” be defined as “having a known
 27 timing relationship with respect to.” Defendants propose that the term be defined as “operating in
 28 step (or in phase) with respect to.”

Defendants' proposed construction suffers from two principal defects. First, the requirement that two signals be "in phase" in order to be considered synchronous with respect to one another is contrary to the specification. For example, the specification notes, with respect to Figure 13, that "the outputs **107** and **108** are *synchronized* with the two bus clocks." '916 patent, col. 23:21-22 (emphasis added). There can be no dispute that to be "synchronized" means the same thing as to behave "synchronously with respect to." See *Coordinated Actions* CC Order at 52-53 (considering "synchronously with respect to" and "synchronize" together and adopting analogous constructions for the two terms); JCCS, Appendix B-2, *LSI* Dkt. # 95-3, at 7-8 (Defendants supporting evidence, citing dictionary definitions of "synchronization" and "synchronizing" in support of proposed construction of "synchronously with respect to"). However, Figure 13 and its accompanying text make clear that outputs **107** and **108** are not in phase with the two bus clocks with which they are synchronized; rather output **107** is phase-shifted so that its rising and falling edges precede the corresponding edges of Bus Clock1, and output **108** is similarly phase-shifted with respect to Bus Clock2. See '916 patent, col. 23:14-20 (describing adjustment of delay lines so that "output **107** precedes the falling edge **121** of the early bus clock, Clock1 **53**, by an amount of time **128** equal to the delay in input sampler **101**" and similarly for output **108**). That two signals may be synchronous with respect to one another even though they are phase-shifted, rather than in phase, is consistent with the IEEE Dictionary's definition of "synchronous" which requires only the maintenance of a "desired phase relationship" rather than matching phase. Detre Decl., Ex. G (1993 IEEE Dictionary), at 1326; accord Detre Decl., Ex. F (1988 IEEE Dictionary), at 978 (definition of "synchronization" requiring "fixed phase relationship" rather than being in phase).

Second, because the Defendants' proposed construction does not expressly allow for any margin of error, the Defendants may argue that it requires that two signals must be *precisely* in step or in phase in order to be synchronous with respect to one another. This would be contrary to the understanding of one of ordinary skill in the art who would understand that timing relationships cannot be arbitrarily precise, but are "known"—as Rambus's proposed construction provides—within the tolerances of the physical systems at issue. Indeed, one of the objects of the

inventions described in the patent specification is to minimize the margin of error—referred to as “clock skew”—in the timing relationships between certain signals to allow for high-speed operation. *See* ’916 patent, col. 3:29-31 (“Another object of this invention is to provide a clocking scheme to permit high speed clock signals to be sent along the bus with minimal clock skew between devices.”). These margins of error cannot, however, be entirely eliminated as the specification recognizes. *See* ’916 patent, col. 18:16-23 (“To operate at a 2 ns data rate, the transit time on the bus should preferably be kept under 1 ns, to leave 1 ns for the setup and hold time of the input receivers (described below) *plus clock skew*.”) (emphasis added).

Rambus’s proposed construction has previously been agreed to by Rambus’s litigation opponents, strongly suggesting that it is the correct understanding of the term. *See* Detre Decl., Ex. B (*Hynix I JCCS*), at 4; Detre Decl., Ex. E (*Coordinated Actions* CC Order), at 52-53 (noting that Hynix, Micron, Samsung, and Nanya did not dispute Rambus’s proposed construction). Moreover, Rambus’s proposed construction follows Judge Whyte’s previous construction of the term. Detre Decl., Ex. E (*Coordinated Actions* CC Order), at 52-53. The Court should likewise follow that construction here.

V. CONCLUSION

For the reasons stated herein, Rambus submits that the Court should adopt its proposed claim constructions of the claim terms in dispute.

Respectfully Submitted,

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